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A COMPARISON OF HIGH TEMPERATURE PERFORMANCE OF SiC DMOSFETs AND JFETs (PREPRINT)

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Sei-Hyung Ryu, Sumi Krishnaswami, Brett Hull, Bradley Heath, Fatima Husna, James Richmond, Anant Agarwal, and John Palmour (Cree Research, Inc.)
Jim Scofield (AFRL/PRPE)

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Cree Research, Inc.
4600 Silicon Drive
Durham, NC 27703

Electrical Technology and Plasma Physics Branch (AFRL/PRPE)
Power Division
Propulsion Directorate
Air Force Research Laboratory, Air Force Materiel Command
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14. ABSTRACT
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A Comparison of High Temperature Performance of SiC DMOSFETs and JFETs

Sei-Hyung Ryu[a], Sumi Krishnaswami[a], Brett Hull[a], Bradley Heath[a], Fatima Husna[a], James Richmond[a], Anant Agarwal[a], John Palmour[a], and James Scofield[b]

[a]Cree, Inc., 4600 Silicon Dr., Durham, NC 27703 USA

sei-hyung_ryu@cree.com, (919) 313-5541, Fax: (919) 313-5696

[b]Air Force Research Laboratory, Wright-Patterson Air Force Base, OH 45433

Keywords: High temperature, High voltage, MOSFET, JFET.

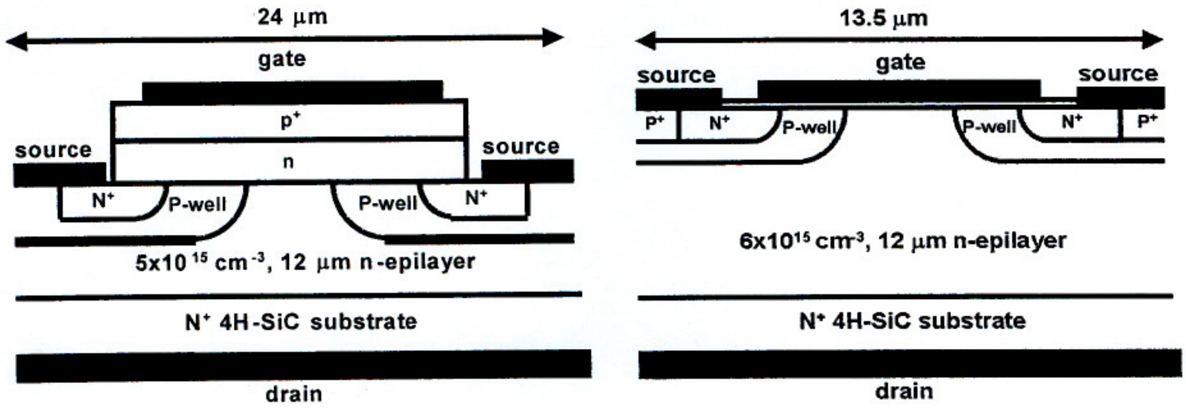
Abstract. High temperature characteristics of 4H-SiC power JFETs and DMOSFETs are presented in this paper. Both devices are based on pn junctions in 4H-SiC, and are capable of 300°C operation. The 4H-SiC JFET showed very predictable, well understood temperature dependent characteristics, because current conduction depends on the drift of electrons in the bulk region, which is not restricted by traps in the MOS interface or pn junctions. However, in a 4H-SiC DMOSFET, electrons must flow through the MOS inversion layer with very high interface state density. At high temperatures, transconductance of the device improves and threshold voltage shifts negative because less electrons are trapped in the interface states, resulting in a much lower MOS channel resistance. This cancels out the increase in drift layer resistance, and as a result, a temperature insensitive on-resistance can be demonstrated. Performances of the two devices are compared, and a discussion of issues for high temperature applications is presented.

Introduction

Silicon Carbide is a very attractive material for high temperature devices. Due to its wide bandgap, the carrier generation in silicon carbide is negligible for temperatures up to 300°C, which results in a very small leakage current in a reverse biased pn junction. Therefore, junction isolation is sufficient for high temperature operations of silicon carbide electronic devices, while dielectric isolation must be used in high temperature silicon devices. This is a significant advantage for silicon carbide because several high voltage power device structures, most of which are vertical devices based on the PiN structure, can be developed for high temperature applications, where only SOI based lateral device structures are available in silicon.

4H-SiC power MOSFETs have attracted a lot of attention because it offers normally-off operations and high impedance gate, which is much easier to control. However, operating temperature of a 4H-SiC power MOSFET is limited to 200°C due to poor reliability of the gate oxide at elevated temperatures. In addition, the specific on-resistance values of the 4H-SiC MOSFETs are relatively high due to extremely low MOS channel mobility. On the other hand, the operation of a 4H-SiC JFET does not depend on gate dielectric. Hence, the operating temperature of a 4H-SiC JFET can be much higher than that of a 4H-SiC MOSFET. In addition, transconductance values in 4H-SiC JFETs are much higher than those in 4H-SiC MOSFETs. Therefore, the JFET channel resistance accounts for only a small fraction of the total on-resistance. However, JFETs are typically normally-on devices, which is not a desirable feature for many power system designers.

In this paper, characteristics of 4H-SiC power MOSFETs and JFETs are presented. Both devices are capable of blocking high voltages, in excess of 600 V. On-state characteristics and blocking



(a) (b)

Fig. 1. Simplified cross-sections (a) of a 4H-SiC JFET, and (b) of a 4H-SiC DMOSFET.

characteristics are measured for temperatures ranging from room temperature to 300°C. Temperature dependence of the on-resistances and leakage currents, as well as overall performances are being compared for the two device types.

Device Structures

Figure 1 shows the simplified cross-sections of a 4H-SiC power JFET and a 4H-SiC DMOSFET. The two structures look very similar because both are based on implanted p-wells. The difference between the two structures is in the formation of lateral channels. In the 4H-SiC JFET, an n-type epilayer is grown on the p-wells to form the lateral channel regions, whereas in the 4H-SiC DMOSFETs, MOS inversion channel layers on the p-wells are utilized instead.

The 4H-SiC JFET is turned on when the top gate is shorted to the source. Electrons flow from the source contact into the n+ source regions, then flow laterally through the lateral JFET channel. The electrons then flow through vertical JFET regions, which are formed by two adjacent p-well regions, through the lightly doped drift layer, and then finally, to the drain contact. The thickness of the lateral JFET channel is defined by the thickness of the n-epilayer and the widths of depletion regions formed by the n-channel and p-well (bottom), and the n-channel and top p+ gate (top). To turn the device off, a negative voltage is applied to the top gate (with respect to the source) and the depletion expands. The device is completely off when the top depletion region touches the bottom depletion, pinching-off the n-channel layer. The 4H-SiC DMOSFET operates in a similar way. The device is turned on when a positive gate bias (greater than the threshold voltage) is applied, and an inversion layer forms under the gate oxide. The device is turned off when the gate bias falls below the threshold voltage, at which the inversion channel disappears.

Device Characteristics

Figure 2 shows the room temperature I-V characteristics of a 4H-SiC JFET. The active area of the device was 0.0465 cm^2. An epilayer with a doping concentration of 5x10^{15}cm^{-3} and a thickness of 12 μm was used as drift layer, and a cell pitch of 24 μm was used. With a V_{GS} of 0 V, a specific on-resistance ($R_{on,sp}$) of 10 mΩ-cm^2, and an on-current of 10 A (=215 A/cm^2) were measured at a forward drop of 2.25 V. The device was able to block 1.8 kV with –33 V on the gate. The theoretical parallel plate E-field of the drift epilayer at this voltage is calculated to be 2.1 MV/cm. Fig. 3 shows the $R_{on,sp}$, measured at a V_{DS} of 0.2 V and a V_{GS} of 0 V, as a function of temperature. The $R_{on,sp}$ increased by a factor of 5 to 50 mΩ-cm^2 at 300°C. This is due to increase in drift layer

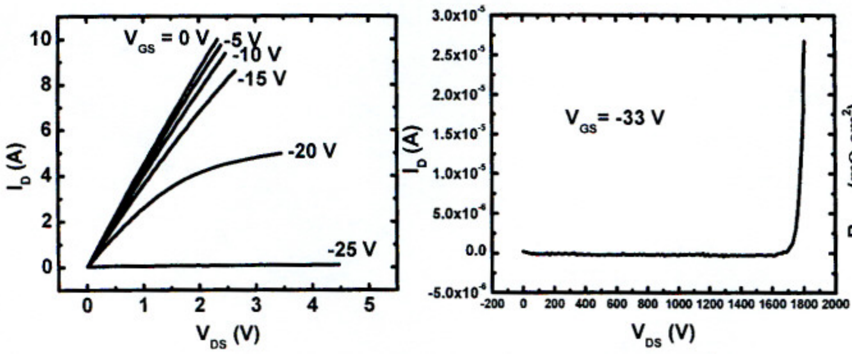


Fig. 3. On-state and blocking characteristics of a 0.0465 cm^2 4H-SiC JFET.

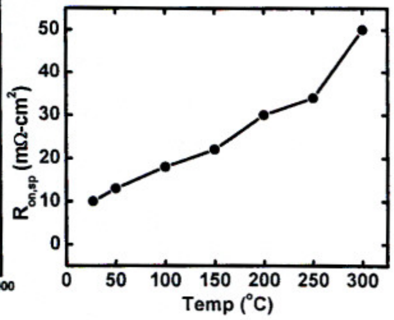


Fig. 4. $R_{on,sp}$ of the 0.0465 cm^2 4H-SiC JFET as a function of temperature.

resistance caused by a decrease in bulk electron mobility [1], and a factor of 10 increase in $R_{on,sp}$ is in good agreement with previously published data on carrier mobility in 4H-SiC [2].

Figure 4 shows the room temperature I-V characteristics of a 4H-SiC DMOSFET. The active area of the device was 0.0276 cm^2. An epilayer with a doping concentration of 6x10^{15}cm^{-3} and a thickness of 12 μm was used as drift layer, which is very close to that used for the JFETs. To compensate for a low MOS channel mobility, a high density design was used for the 4H-SiC DMOSFETs, which resulted in a much tighter cell pitch of 13.5 μm. A $R_{on,sp}$ of 11 mΩ-cm^2 was measured with a V_{DS} of 1 V and a V_{GS} of 15 V, which corresponds to a gate oxide E-field of 3.0 MV/cm. An on-current of 5 A (=181 A/cm^2), was observed at a V_{DS} of 1.9 V. The device showed stable avalanche characteristics at a V_{DS} of 2 kV with a V_{GS} of 0 V. Fig. 6 shows the $R_{on,sp}$ of the 4H-SiC DMOSFET as a function of temperature. The $R_{on,sp}$ increased by a factor of 2, to 20 mΩ-cm^2 at 300°C. The MOS channel resistance in the 4H-SiC DMOSFET, with a fixed gate bias (V_{GS} =15 V), decreases at elevated temperatures because of the negative shifts in threshold voltage and the increases in MOS channel mobility [3]. The decrease in the MOS channel resistance cancels out the increase in drift layer resistance. As a result, 4H-SiC DMOSFETs can exhibit temperature insensitive $R_{on,sp}$. It should also be noticed that the $R_{on,sp}$ of the 4H-SiC DMOSFET is much lower than that of the 4H-SiC JFET at 300°C. This is due to the tighter cell pitch of the DMOSFET, which also reduces the vertical JFET resistance and spreading resistance of the structure [4].

Figure 6(a) shows the leakage current of the 4H-SiC JFET in the off-state for temperatures ranging from room temperature to 300°C. A V_{GS} of –33 V was used for the measurements. The drain voltage was limited to 600 V due to limitation in the package. For temperatures up to 250°C, the leakage current at 600 V remained at around 0.1 μA, which increased to approximately 1.5 μA, which corresponds to a current density of approximately 32 μA/cm^2, at 300°C. This suggests that

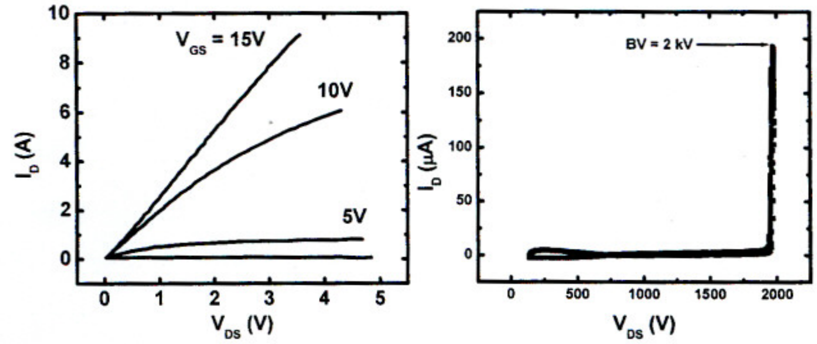


Fig. 5. On-state and blocking characteristics of a 0.0276 cm^2 4H-SiC DMOSFET.

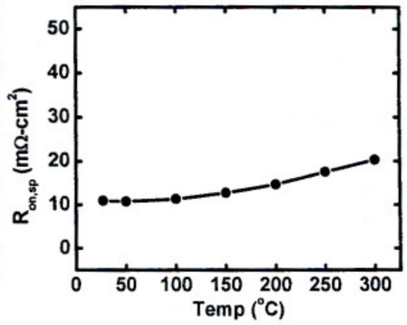
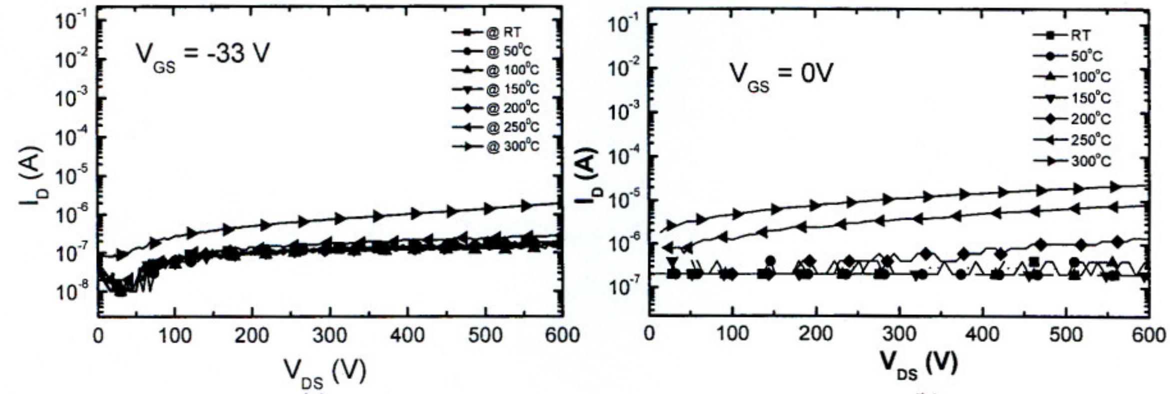


Fig. 6. $R_{on,sp}$ of the 0.0276 cm^2 4H-SiC DMOSFET as a function of temperature.



(a) (b)

Fig. 7. Blocking characteristics of (a) the 4H-SiC JFET and (b) the 4H-SiC DMOSFET.A maximum drain bias of 600 V was used, and a V_{GS} of –33 V was used for the JFET and a V_{GS} of 0 V was used for the DMOSFET.

the JFET can be safely operated at temperatures up to 300°C. Fig. 6(b) shows the off-state characteristics of the 4H-SiC DMOSFET. A V_{GS} of 0 V was used for the measurement. The DMOSFET leakage current was comparable to that of the JFET at low temperatures, a significantly higher leakage current was observed for temperatures above 200°C. This result suggests that although the 4H-SiC DMOSFET can provide acceptable performances, 4H-SiC JFETs are preferred devices for high temperature applications.

Summary

SiC devices are capable of high temperature operation due to the very wide bandgap and low leakage current in the reverse biased pn junctions. Two types of power switching devices – JFETs and DMOSFETs – were presented in this paper. The 4H-SiC JFET demonstrated excellent high temperature characteristics, and showed very stable operations for temperatures up to 300°C. 4H-SiC DMOSFET showed a temperature insensitive on-resistance, which makes the device very attractive for switch mode power supply applications, and demonstrated its capability to operate at 300°C. However, the increased leakage current of the 4H-SiC DMOSFETs indicates that the 4H-SiC JFETs are the preferred devices for high temperature applications. With use of suitable circuit topology and further development of fabrication technology, these two devices can enable high performance, high temperature power electronic applications which are not possible with devices in conventional semiconductor materials.

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